REMARKS

Claims 1 – 19 are pending and rejected.

The applicants' attorney has amended claims 1, 9 and 15 not to overcome the examiner's rejection, but to more clearly recite and aspect of the applicants' invention. The applicants' attorney respectfully disagrees with the examiner's rejection of claims 1 – 19 and asserts that the claims, as amended, are in condition for allowance for the reasons discussed below.

Rejection of Claims 1 – 8 under 35 U.S.C. §102(b)

The applicants' attorney disagrees with the examiner's rejection of claim 1 over U.S. patent 5,646,828 issued to Degani *et. al.* (Degani) because Degani fails to disclose an interconnection substrate having a surface area smaller than the surface area of the semiconductor substrate that the interconnection substrate is mounted on.

The applicants' claim 1, as amended, recites an integrated circuit comprising a semiconductor substrate having a circuit and a surface area, and an interconnection substrate mounted on the semiconductor substrate and having a surface area smaller than the semiconductor substrate surface area.

For example, as shown in FIG. 2 and discussed in paragraphs 15, 21, 23, 26 and 25 of the specification, an integrated circuit device 50 includes a substrate 60, a semiconductor substrate 54, and an interconnection substrate 70 that may distribute power and ground within the semiconductor substrate 54. The semiconductor substrate 54 includes a circuit (not shown in FIG. 2). The interconnection substrate 70 is connected to the substrate 60 by wire bonds 67 and connected to the semiconductor substrate 54 by solder balls 72. Some of the electrical signals from the substrate 60 to the semiconductor substrate 54, and vice versa, travel through the interconnection substrate 70. The interconnection substrate 70 includes a surface area, which the semiconductor substrate 54 is bonded to, that is smaller than the surface area of the semiconductor substrate 54, which the interconnection substrate 70 bonds to. By reducing the surface area of the interconnection substrate 70 to less than the surface area of the semiconductor substrate 54, wire bonds 66 may connect the substrate 60 to the semiconductor substrate 54 to allow other electrical signals to travel from the substrate 60 to the semiconductor substrate 54, and vice versa, without traveling through the interconnection substrate 70.

In contrast, Degani fails to disclose an interconnection substrate having a surface area smaller than the surface area of the semiconductor substrate that the interconnection substrate is mounted on. Degani discloses a multi-chip module (MCM) package 35 (FIG. 2) that includes an MCM tile 17 (FIG. 2) connected to a printed wiring board (PWB) 36 (FIG. 2). The MCM tile 17 includes a silicon substrate 18 and silicon chips 19 and 20. The silicon substrate 18 is an interconnection substrate (*See Col. 3 lines 55 – 63*) and the chips 19 and 20 include an integrated circuit (*See Col. 3 lines 55 – 63*). The chips 19 and 20 are connected to the silicon substrate 18 by solder balls (shown without a reference number) that allow electrical signals to travel between the substrate 18, chip 19 and chip 20. The silicon substrate 18 is connected to the PWB 36 by wires 22 that allow electrical signals to travel between the substrate 18 and the PWB 36. Electrical signals from the PWB 36 to the chips 19 and 20, and vice versa, travel through the silicon substrate 18. The silicon substrate 18 (interconnection substrate) includes a surface area, to which the chips 19 and 20 are bonded, that is larger than the surface area of each chip 19 and 20, to which the silicon substrate 18 bonds. Degani fails to disclose that the silicon substrate 18 (interconnection substrate) has a circuit, and therefore, the silicon substrate 18 is not analogous to the applicants' semiconductor substrate 54, which does include a circuit. Therefore, unlike the applicants' claimed interconnection substrate, the surface area of the silicon substrate 18 is larger than the surface area of the chip 19, or the surface area of the chip 20; not smaller.

Claims 2 – 8 are patentable by virtue of their dependencies on claim 1.

Rejection of Claims 9 – 14 under 35 U.S.C. §102(b)

Claim 9 is patentable over Degani for reasons similar to those recited above in support of claim 1 over Degani.

Claims 10 - 14 are patentable by virtue of their dependencies from claim 9.

Rejection of Claims 15 – 19 under 35 U.S.C. §102(b)

Claim 15 is patentable over Degani for reasons similar to those recited above in support of claim 1 over Degani.

Claims 16 – 19 are patentable by virtue of their dependencies from claim 15.

Conclusion

The applicants' attorney respectfully requests the examiner withdraw the rejection of claims 1 – 19 in view of the remarks above and issue an allowance for these claims.

If the examiner believes that a phone interview would be helpful, he is respectfully requested to contact the applicants' attorney, John Janeway, at (425) 455-5575.

DATED this 25th day of April 2005.

Respectfully submitted,

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